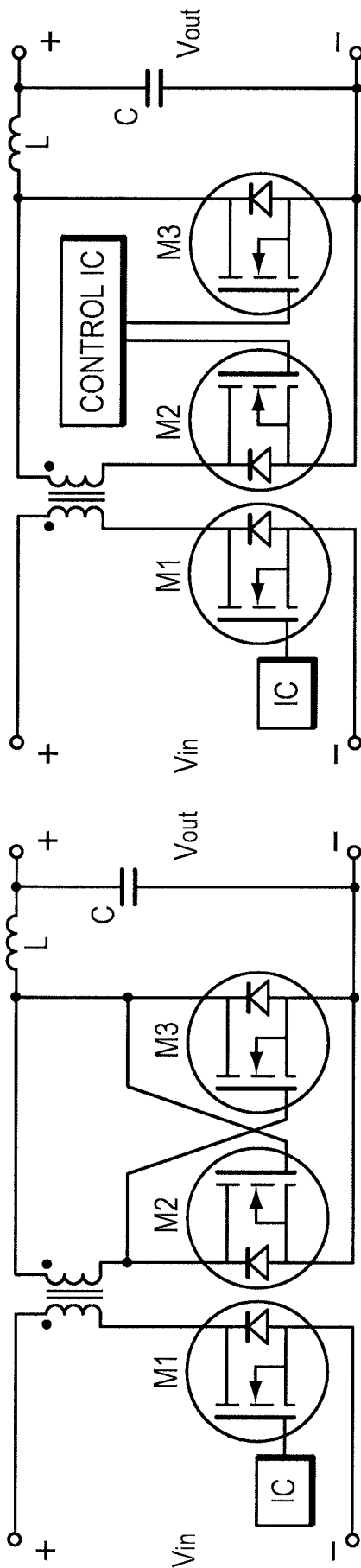


+



IC-DRIVEN SYNCHRONOUS RECTIFICATION
ISOLATED FORWARD CONVERTER

FIG. 1B

SELF-DRIVEN SYNCHRONOUS RECTIFICATION
ISOLATED FORWARD CONVERTER

FIG. 1A

+

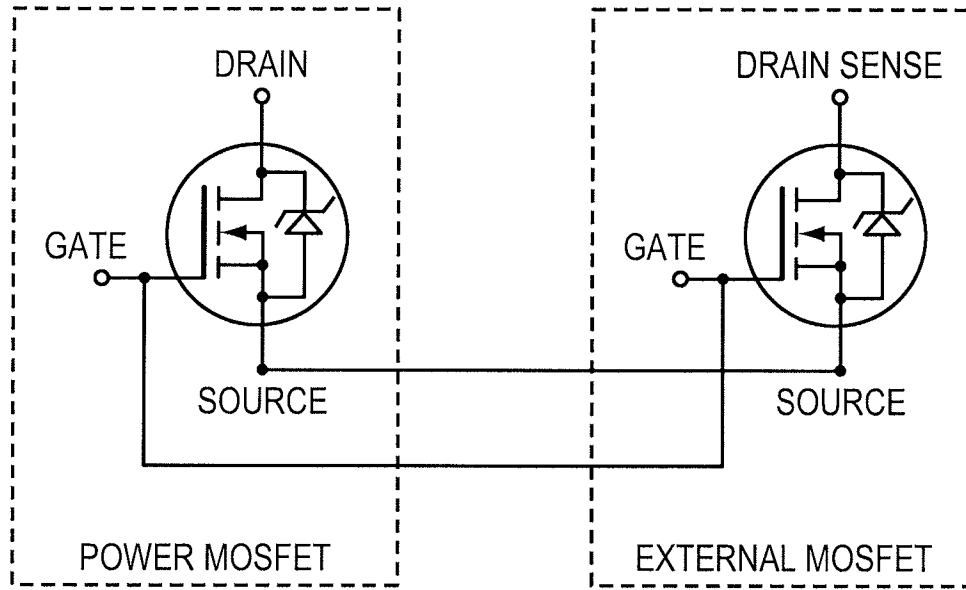
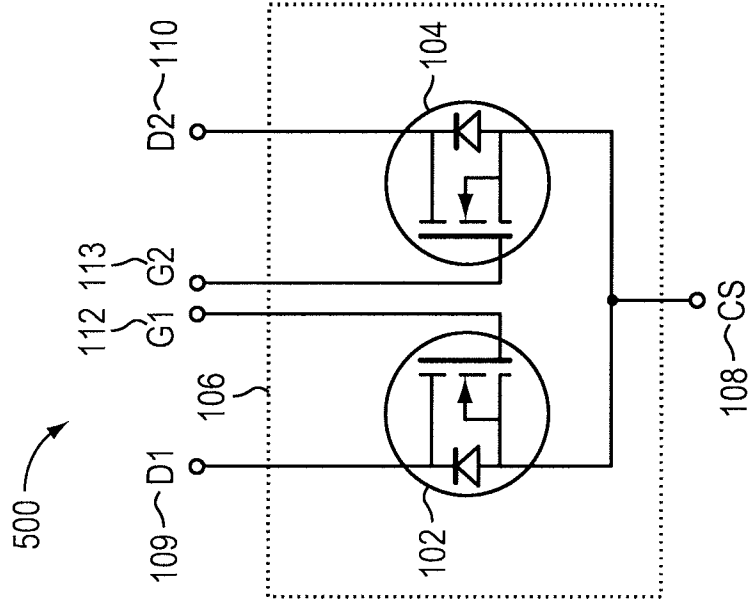
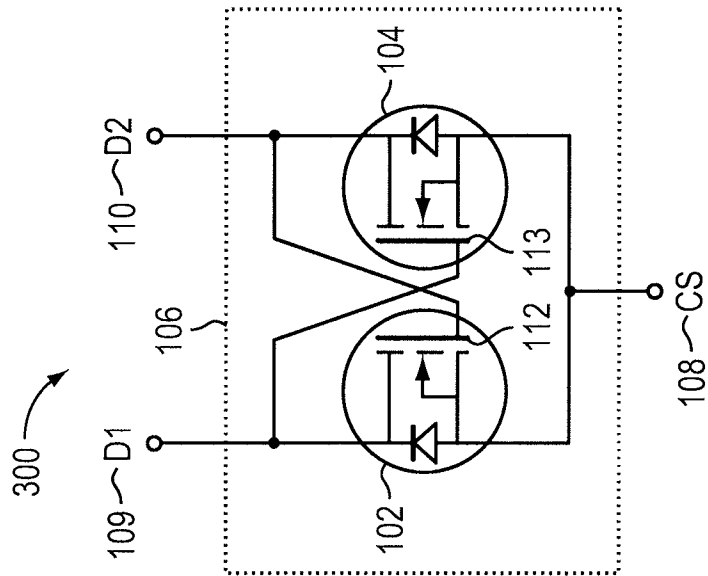


FIG. 2



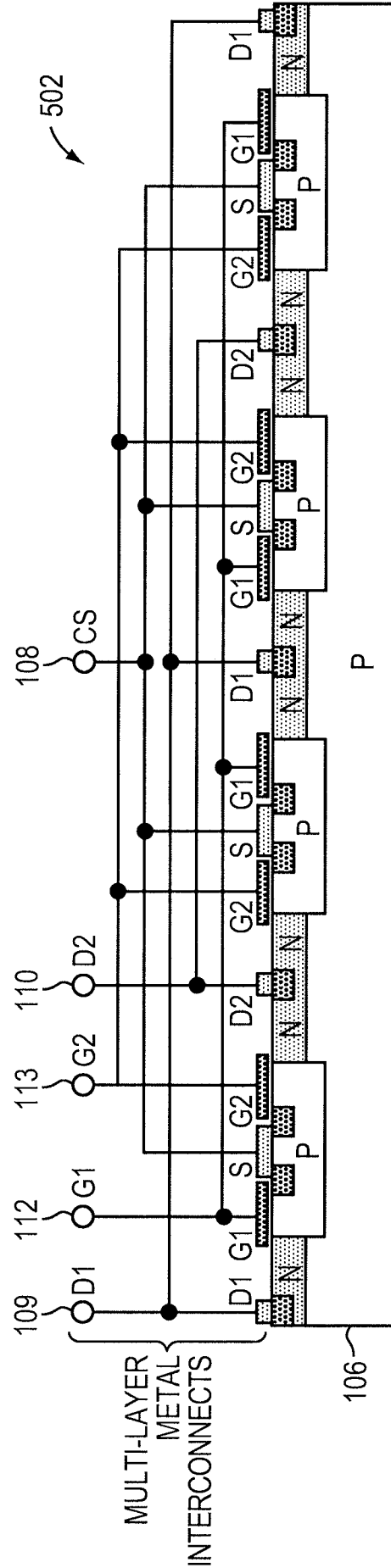
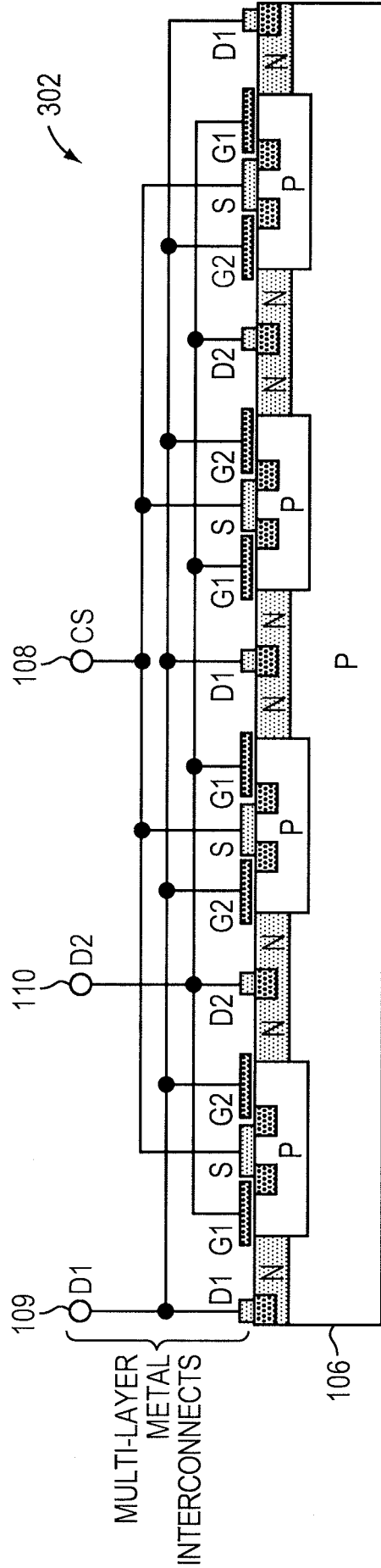
SECOND EMBODIMENT:
 5-LEAD CONTROL IC-DRIVEN
 SYNCHRONOUS RECTIFICATION
 MOSFET PAIR

FIG. 3B



FIRST EMBODIMENT:
 3-LEAD SELF-DRIVEN
 SYNCHRONOUS RECTIFICATION
 MOSFET PAIR

FIG. 3A



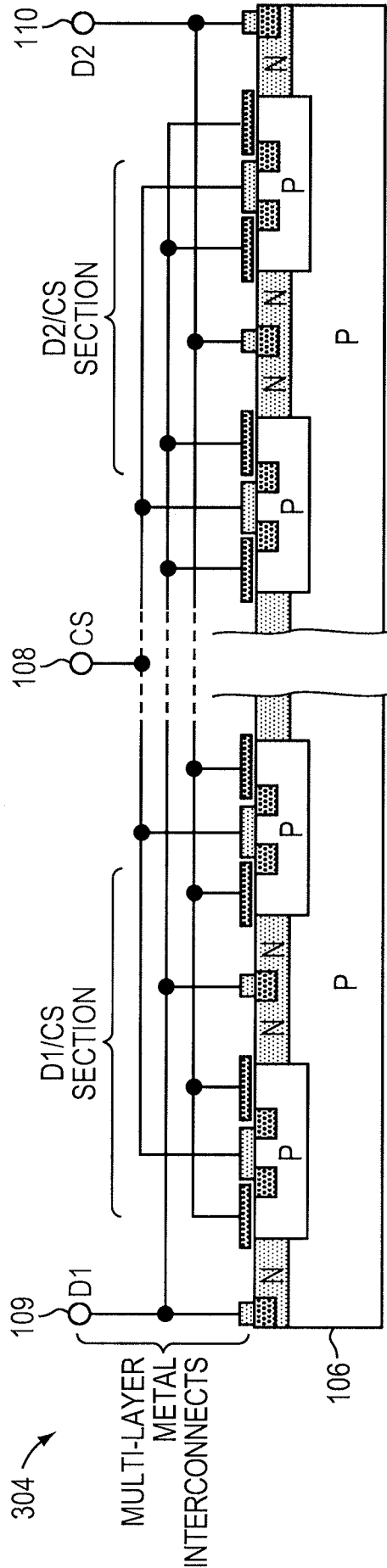


FIG. 5A

THIRD EMBODIMENT: 3-LEAD SELF-DRIVEN MOSFET PAIR IN SEPARATE CELL SECTIONS

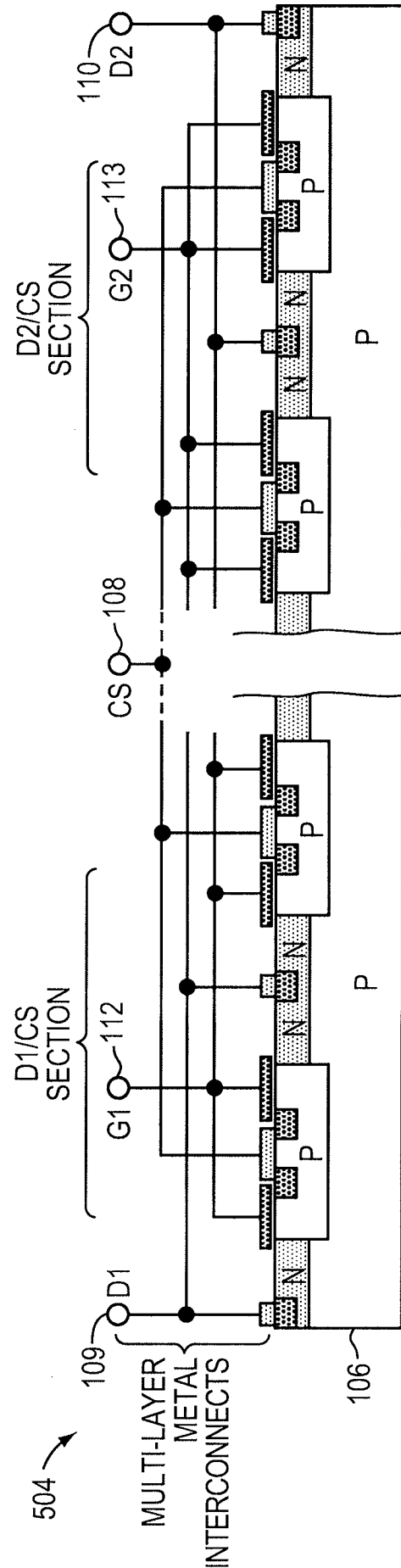


FIG. 5B

FOURTH EMBODIMENT: 5-LEAD EXTERNAL-DRIVEN MOSFET PAIR IN SEPARATE CELL SECTIONS

1. DISCRETE POWER SEMICONDUCTOR DEVICE COMPRISED
OF MULTIPLE TRANSISTORS WITH COMMON SOURCE CONNECTION
WITH ONE OR MORE TRANSISTORS HAVING
ELECTRICALLY ISOLATED DRAIN AND GATE CONNECTIONS

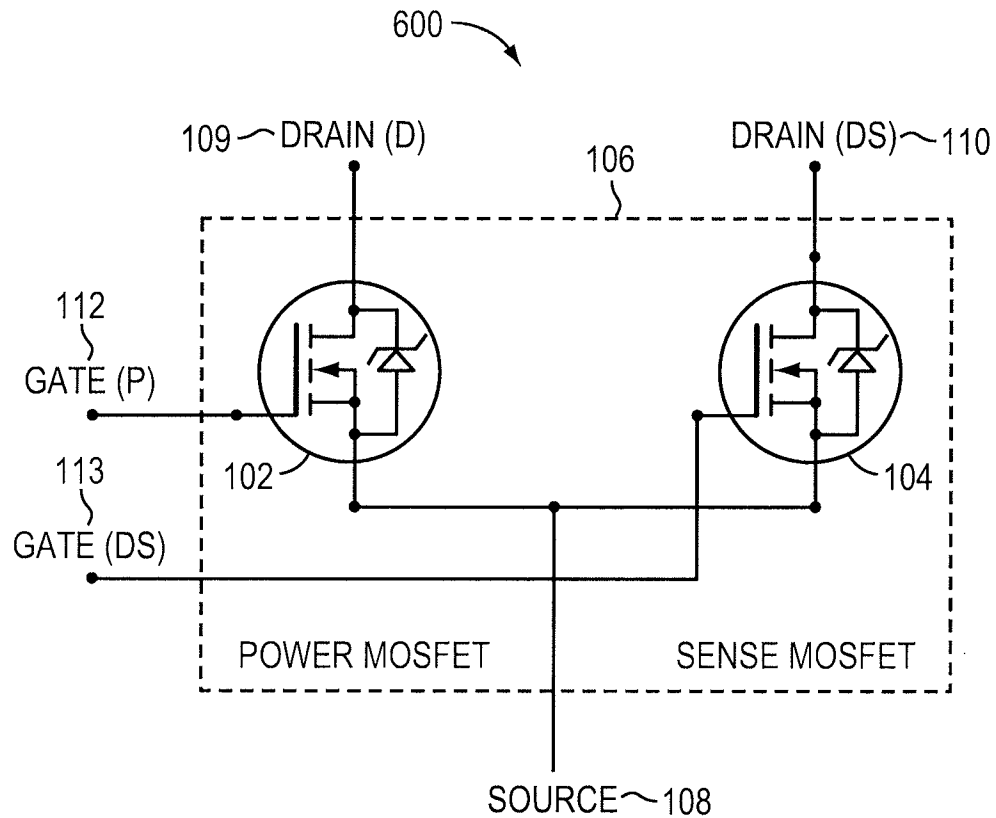


FIG. 6

+

1. DISCRETE POWER SEMICONDUCTOR DEVICE COMPRISED OF MULTIPLE TRANSISTORS
WITH COMMON SOURCE CONNECTION WITH ONE OR MORE TRANSISTORS HAVING
ELECTRICALLY ISOLATED DRAIN AND GATE CONNECTIONS

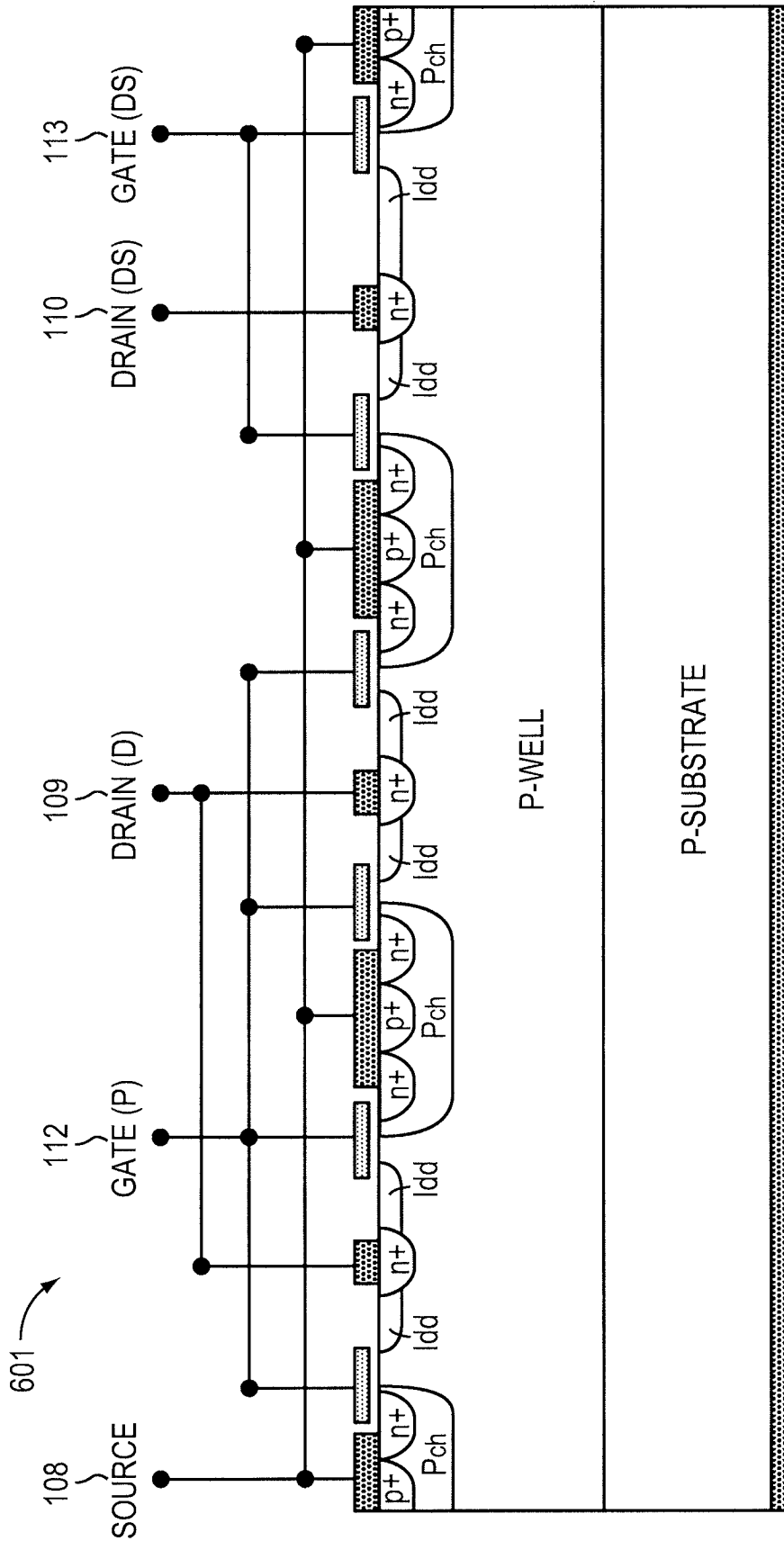


FIG. 7
CROSS-SECTIONAL DIAGRAM OF A POWER MOSFET WITH INTEGRATED DRAIN SENSE

+

2. DISCRETE POWER SEMICONDUCTOR DEVICE COMPRISED
OF MULTIPLE TRANSISTORS WITH COMMON SOURCE AND
GATE CONNECTIONS WITH ONE OR MORE TRANSISTORS HAVING
ELECTRICALLY ISOLATED DRAIN CONNECTIONS

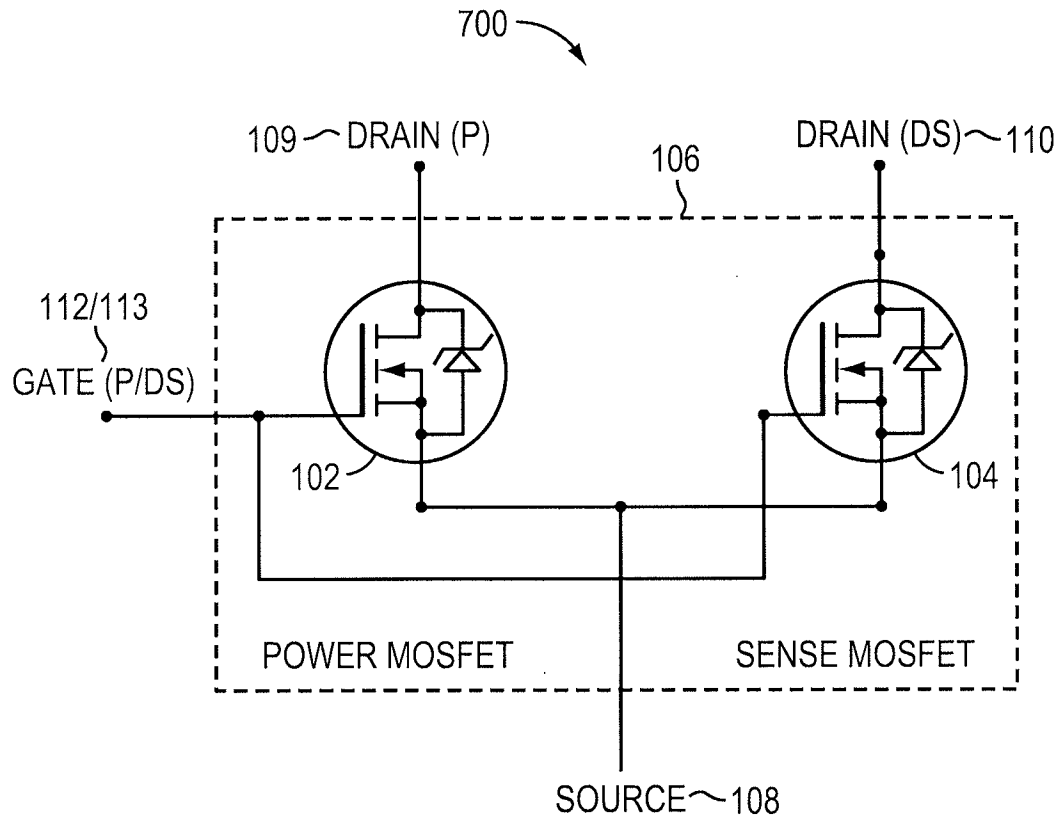


FIG. 8

+

2. DISCRETE POWER SEMICONDUCTOR DEVICE COMPRISED OF MULTIPLE TRANSISTORS
 WITH COMMON SOURCE AND GATE CONNECTIONS WITH ONE OR MORE TRANSISTORS
 HAVING ELECTRICALLY ISOLATED DRAIN CONNECTIONS

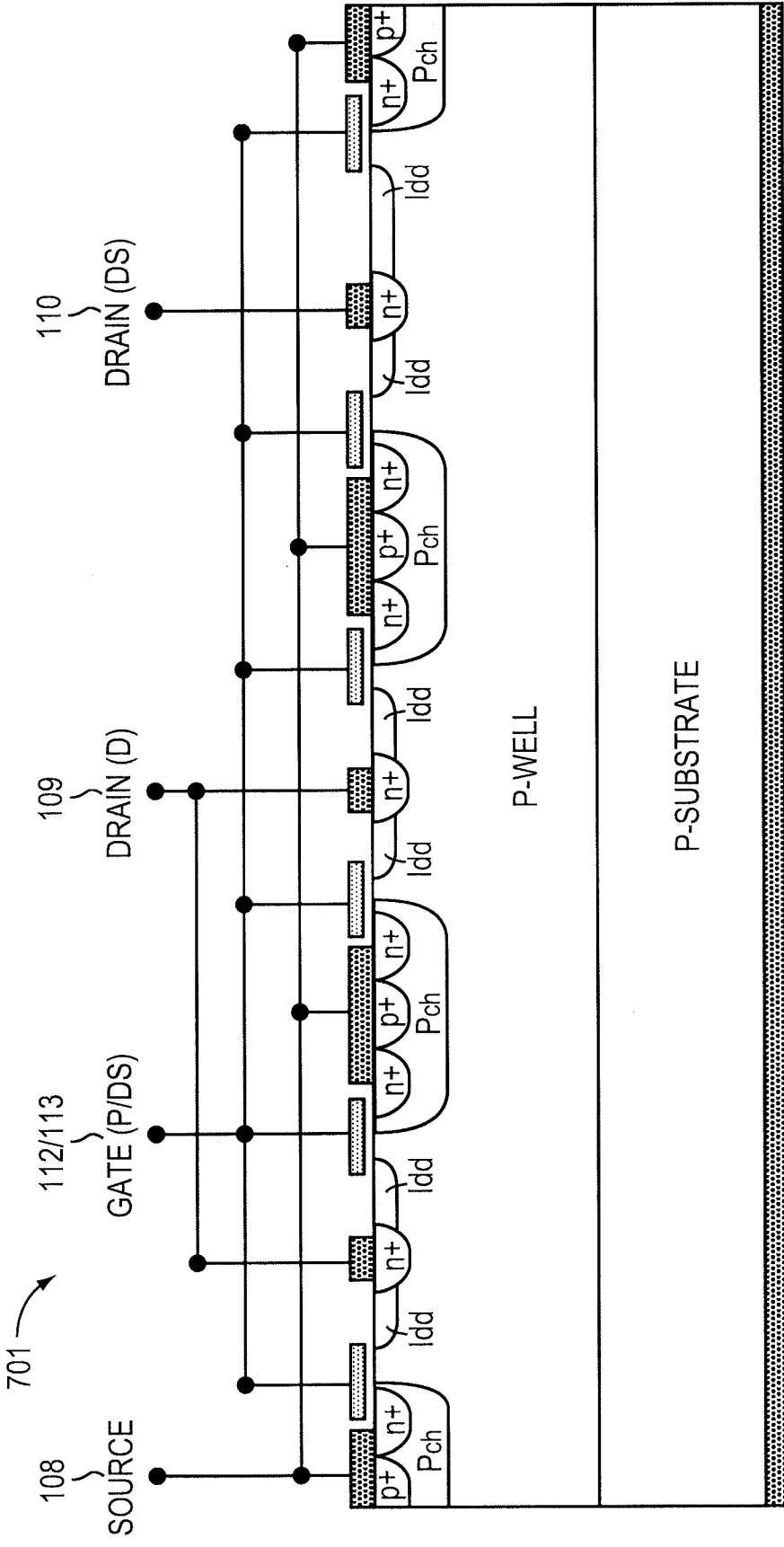


FIG. 9
 CROSS-SECTIONAL DIAGRAM OF A POWER MOSFET WITH INTEGRATED DRAIN SENSE

+



3. DISCRETE POWER SEMICONDUCTOR DEVICE COMPRISED
OF MULTIPLE TRANSISTORS WITH COMMON SOURCE AND
GATE CONNECTIONS WITH ONE OR MORE TRANSISTORS HAVING
SUBSTANTIALLY DIFFERENT THRESHOLD VOLTAGES
AND ELECTRICALLY ISOLATED DRAIN CONNECTIONS

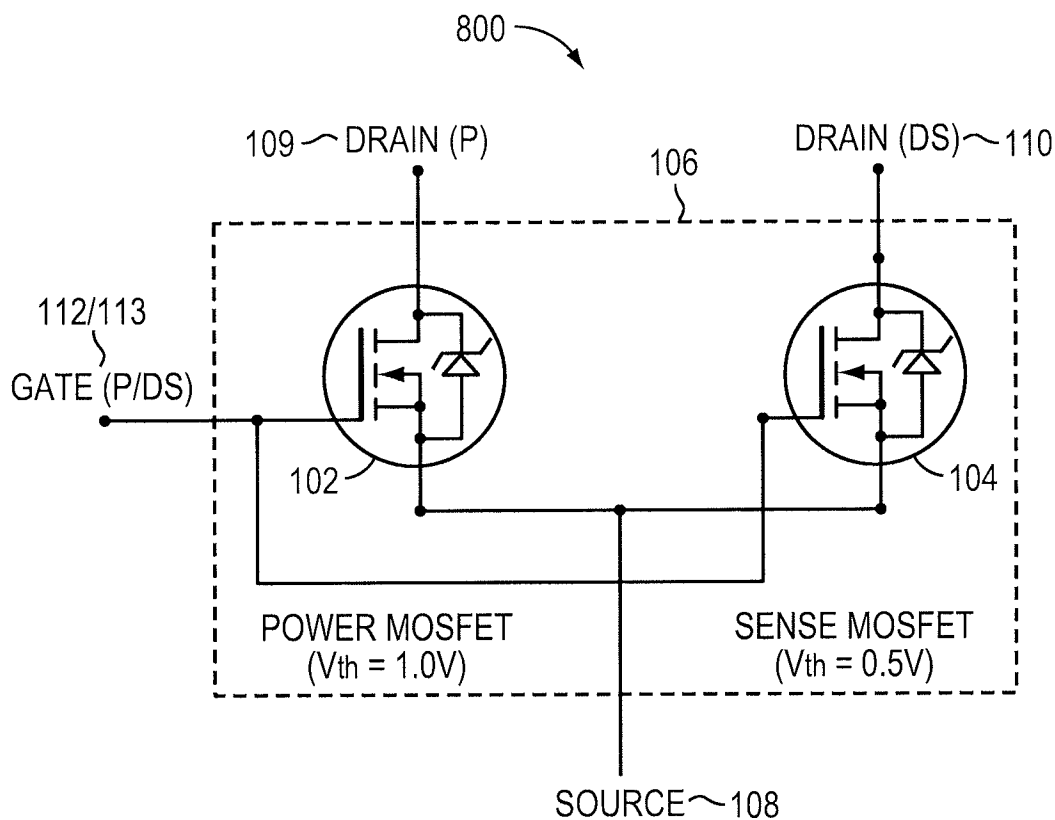


FIG. 10



3. DISCRETE POWER SEMICONDUCTOR DEVICE COMPRISED OF MULTIPLE TRANSISTORS
WITH COMMON SOURCE AND GATE CONNECTIONS WITH ONE OR MORE TRANSISTORS
HAVING SUBSTANTIALLY DIFFERENT THRESHOLD VOLTAGES
AND ELECTRICALLY ISOLATED DRAIN CONNECTIONS

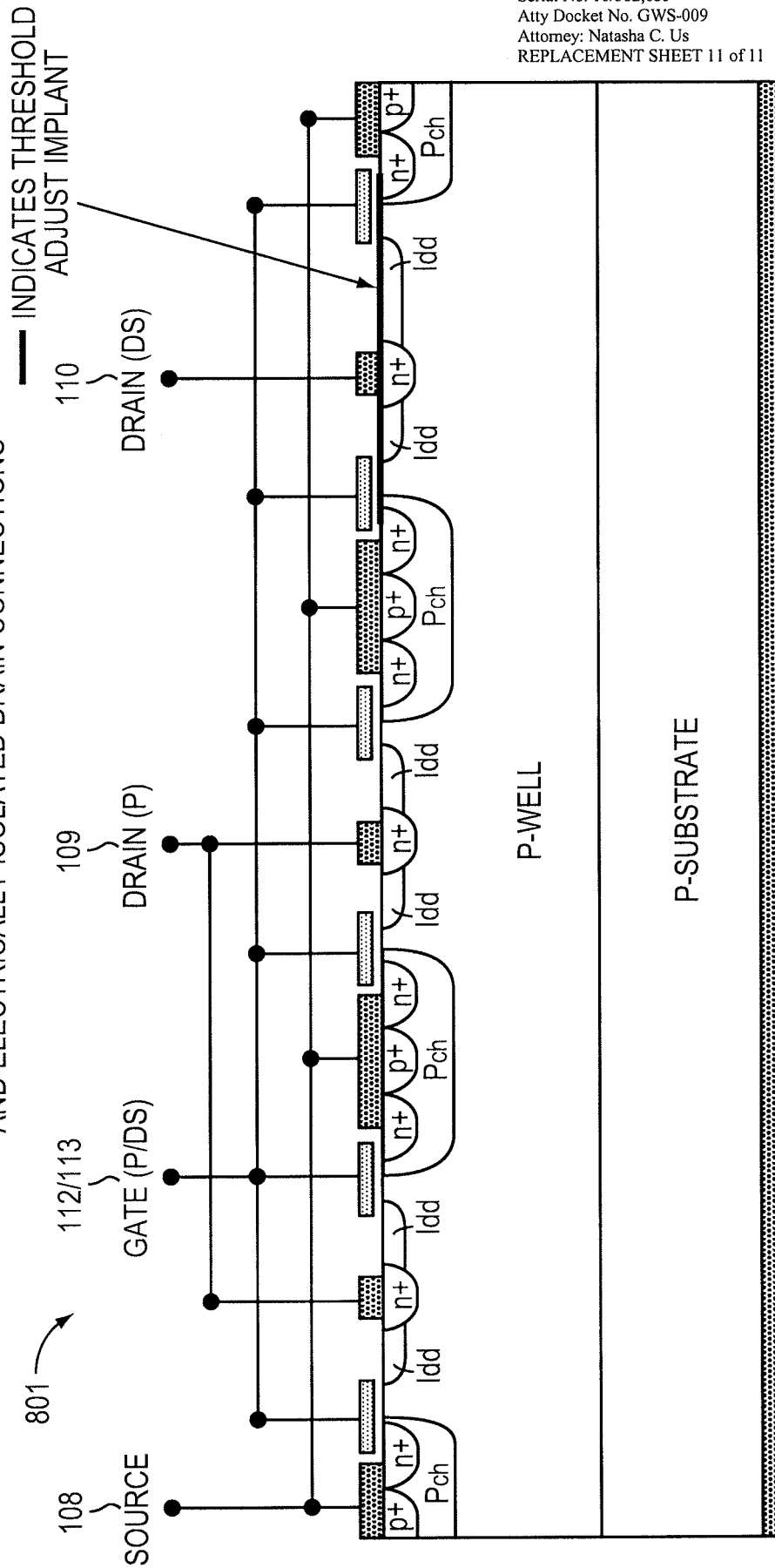


FIG. 11
CROSS-SECTIONAL DIAGRAM OF A POWER MOSFET WITH INTEGRATED DRAIN SENSE

